# AN1048
# Application note

## ST7 software LCD driver

## Introduction

This note describes a technique for driving Liquid Crystal Displays (LCD) with any standard ST7 Microcontroller (MCU) i.e without any specific on-chip LCD driver hardware. This technique offers a solution for applications which require a display at low cost together with the versatile capabilities of the standard ST7 MCUs. This note also provides a technique to control the LCD contrast through software.

After an introduction on LCDs in *Section 1*, *Section 2* & *3* of this note describes the typical waveforms required to drive an LCD with a multiplexing rate of 1 or 2 (duplex) and 4 (quadruplex). *Section 3* presents a solution based on a standard ST7 MCU directly driving a quadruplex LCD. This solution can be implemented with any ST7 MCU as it only requires the standard I/O ports and one timer, both of which are standard features on all ST7 MCUs. *Section 4* describes how to control the contrast through software. Finally, *Section 5* gives a brief overview of the LCD demo board including the board schematics. The demo board, based on a ST72F321B microcontroller, allows the user to develop and test applications using an LCD device.

The program size (~300 bytes), the CPU load required for controlling the LCD (0.2%), and the number of external components is kept to the minimum (two external resistors per COM line). The number of I/O's is the same as a solution using an on-chip LCD hardware driver or an external hardware LCD driver. With software contrast control, it is a very flexible solution that can be adapted easily to a range of applications.

# Contents


**1 LCD requirements . . . . . 3**

**2 LCD drive signals . . . . . 4**

2.1 Single backplane LCD drive . . . . . 4

2.2 Duplexed LCD drive . . . . . 4

2.3 Quadruplex LCD drive . . . . . 6

2.3.1 LCD mean voltage calculation . . . . . 8

2.3.2 Contrast calculation . . . . . 9

**3 Example of a quadruplex LCD with ST72F321B . . . . . 11**

**4 Software contrast control . . . . . 16**

4.1 Contrast calculations . . . . . 16

**5 LCD demo board . . . . . 18**

5.1 Schematic . . . . . 18

5.2 Power supply . . . . . 19

5.3 Programming . . . . . 19

5.4 Reset . . . . . 19

5.5 Oscillation system . . . . . 19

**6 Revision history . . . . . 20**

# 1 LCD requirements

With a low Root Mean Square (RMS i.e.: $\sqrt{Mean(Signal^2)}$) voltage applied to it, an LCD is practically transparent. The LCD segment is inactive(OFF) if the RMS voltage is below the LCD threshold voltage and is active(ON) if the LCD RMS voltage is above the threshold voltage. The LCD threshold voltage depends on the quality of the liquid used in the LCD and the temperature. The optical contrast is defined by the difference in transparency of a LCD segment ON (dark) and a LCD segment OFF (transparent). The optical contrast depends on the difference between the RMS voltage on an ON segment ($V_{ON}$) and the RMS voltage on an OFF segment ($V_{OFF}$). The higher the difference between $V_{ON}$(rms) and $V_{OFF}$(rms), the higher the optical contrast. The optical contrast also depends on the level of $V_{ON}$ versus the LCD threshold voltage. If $V_{ON}$ is below or close to the threshold voltage, the LCD is completely or almost transparent. If $V_{OFF}$ is close or above the threshold voltage, the LCD is completely dark.

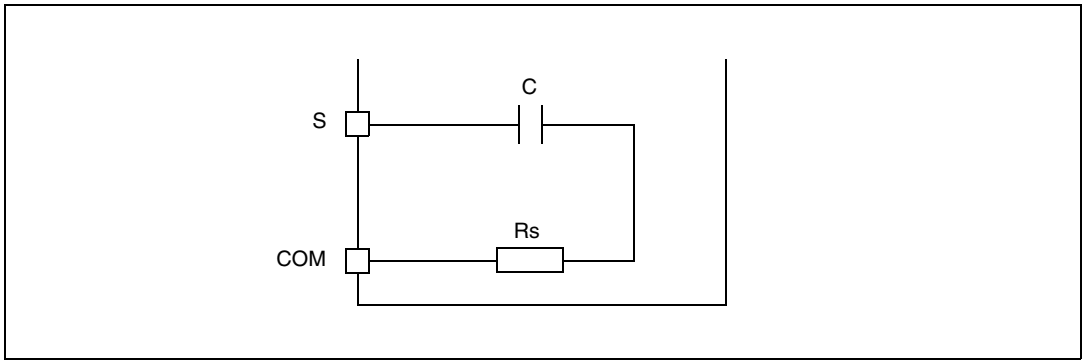
In this document, contrast is defined as D = $V_{ON}$(rms) / $V_{OFF}$(rms).

The applied LCD voltage must alternate to give a zero DC value in order to ensure a long LCD life time.

The higher the multiplexing rates, the lower the contrast. The signal period has also to be short enough to avoid visible flickering on the display.

The LCD voltage for each segment is equal to the difference between the S and COM voltages (see *Figure 1*).

**Figure 1. Equivalent Electrical Schematic of an LCD Segment**




*Note: The DC Value should never be more than 100mV (refer to the LCD manufacturer's datasheet). Otherwise the life time can be shortened. The frequency range is 30 - 200Hz typically. If it is less, it flickers; if it is more, the power consumption increases.*

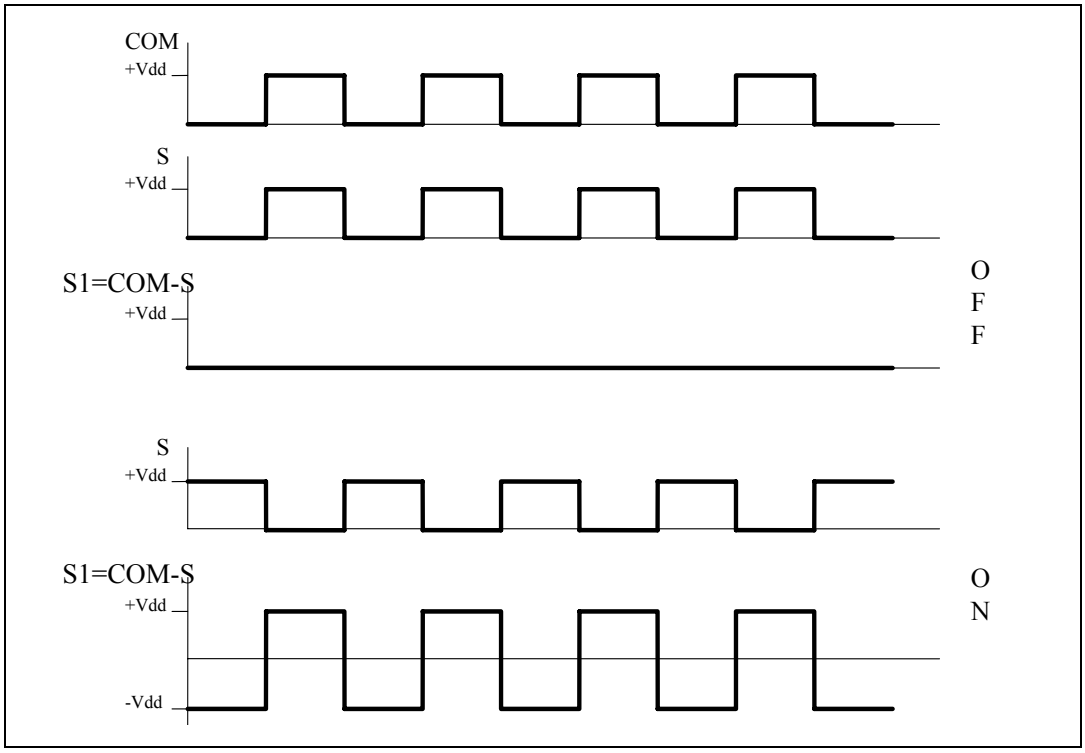
# 2 LCD drive signals

## 2.1 Single backplane LCD drive

In a single backplane drive, each LCD segment is connected to a segment line(Sx) and to one backplane(common line) common to all the segments. A display using S segments is driven with S+1 MCU output lines. The backplane is driven with a “COM” signal controlled between 0 and $V_{DD}$ with a duty cycle of 50%.

When switching a segment “ON”, a signal with opposite polarity to “COM” is sent to the corresponding “Segment” pin. When the non-inverted signal “COM” is sent to the “Segment” pin, the segment is “OFF”. Using an MCU, the I/O operates in output mode either at logic 0 or 1.

**Figure 2. LCD signals for direct drive**




## 2.2 Duplexed LCD drive

In a duplexed drive, two backplanes are used instead of one. Each LCD segment line(Sx) is connected to two LCD segments, each one connected on the other side to one of the two backplanes or common lines(refer to *Figure 3*). Thus, only (S/2)+2 MCU pins are necessary to drive an LCD with S segments.

Three different voltage levels have to be generated on the backplanes: 0, $V_{DD}/2$ and $V_{DD}$. The “Segment” voltage levels are 0 and $V_{DD}$ only. Figure 4 shows typical Backplane, Segment and LCD waveforms. The intermediate voltage $V_{DD}/2$ is only required for the Backplane voltages. The ST7 I/O pins selected as “Backplanes” are set by software to output mode for

0 or $V_{DD}$ levels and to high impedance input mode for $V_{DD}/2$. When one backplane is active, the other one is neutralised by applying $V_{DD}/2$ to it. This $V_{DD}/2$ voltage is defined by two resistors of equal value, externally connected to the I/O pin. By using an MCU with flexible I/O pin configuration, a duplexed LCD drive can be implemented with only 2 external resistors bridge (each on two com lines).

**Figure 3. Basic LCD Segment Connection in duplexed mode**

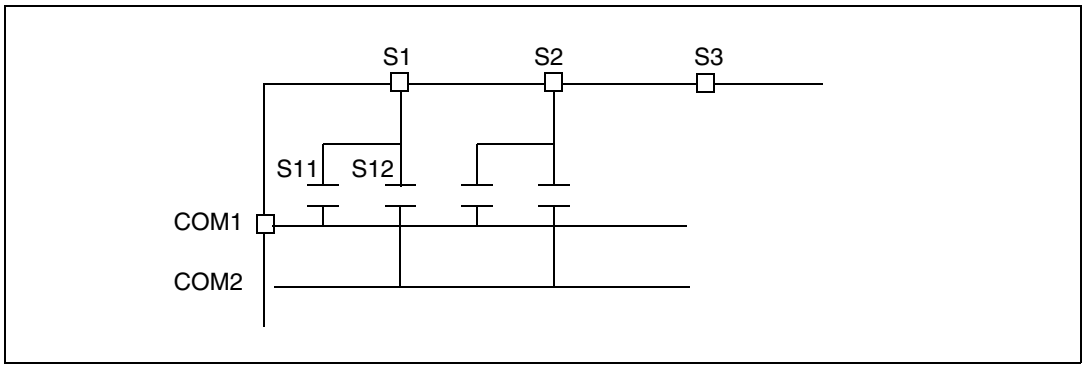
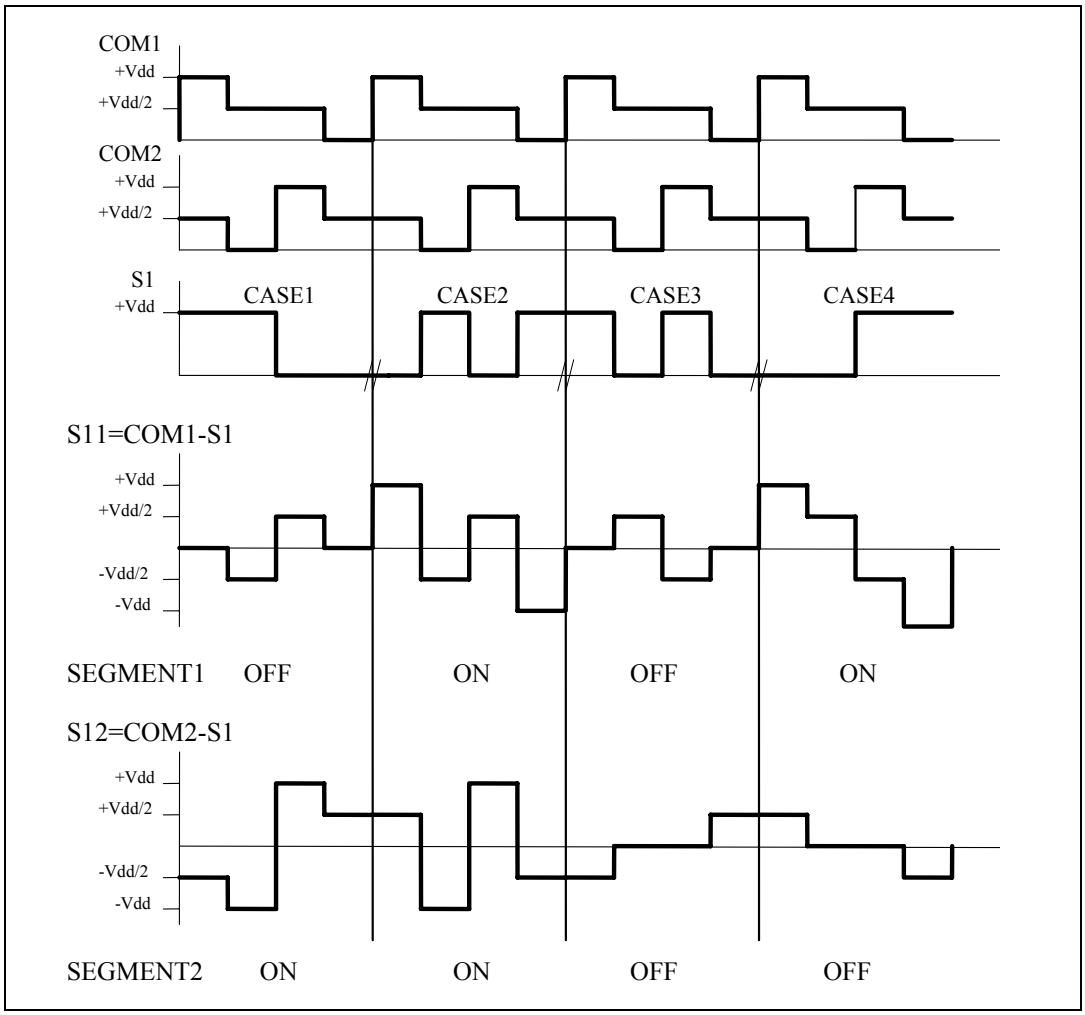



**Figure 4. LCD signals for duplexed mode (used in the ST7 example)**



## 2.3 Quadruplex LCD drive

In a quadruplex LCD drive, four backplanes are used. Each LCD pin is connected to four LCD segments, with each segment connected on the other side to one of the four backplanes. Thus, only (S/4)+4 MCU pins are necessary to drive an LCD with S segments. For example: to drive an LCD with 128 segments (32 x4), only 36 I/O ports are required (32 I/O ports to drive the segments, 4 I/O ports to drive the backplanes).

Three different voltage levels have to be generated on the common lines: 0, $V_{DD}/2$, $V_{DD}$. The Segment line voltage levels are 0 and $V_{DD}$ only. The LCD segment is inactive if the RMS voltage is below the LCD threshold voltage and is active if the LCD RMS voltage is above the threshold. *Figure 6* shows typical Backplane, Segment and LCD waveforms. The intermediate voltage $V_{DD}/2$ is only required for Backplane voltages. The MCU I/O pins selected as “Backplanes” are set by software to output mode for 0 or $V_{DD}$ levels and to the high impedence input mode for $V_{DD}/2$. The $V_{DD}/2$ voltage is defined by two resistors of equal value, externally connected to the I/O pins. When one backplane or COM is active, the other ones are neutralized by applying $V_{DD}/2$ to them.

**Figure 5. Basic LCD Segment Connection in Quadruplexed Mode**

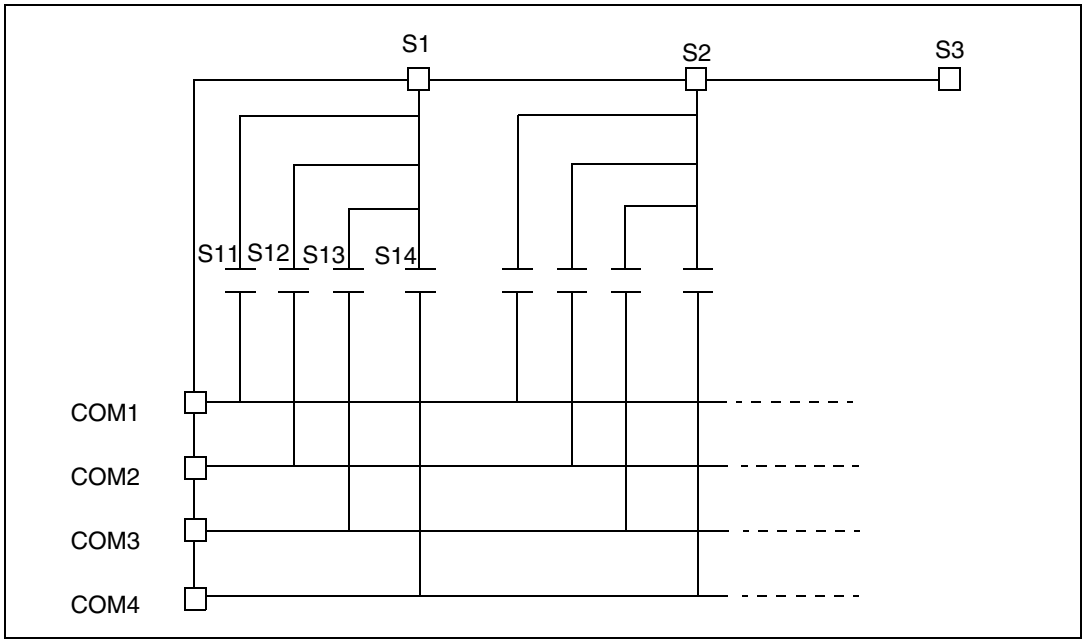


**Figure 6. LCD timing diagram for Quadruplex Mode**

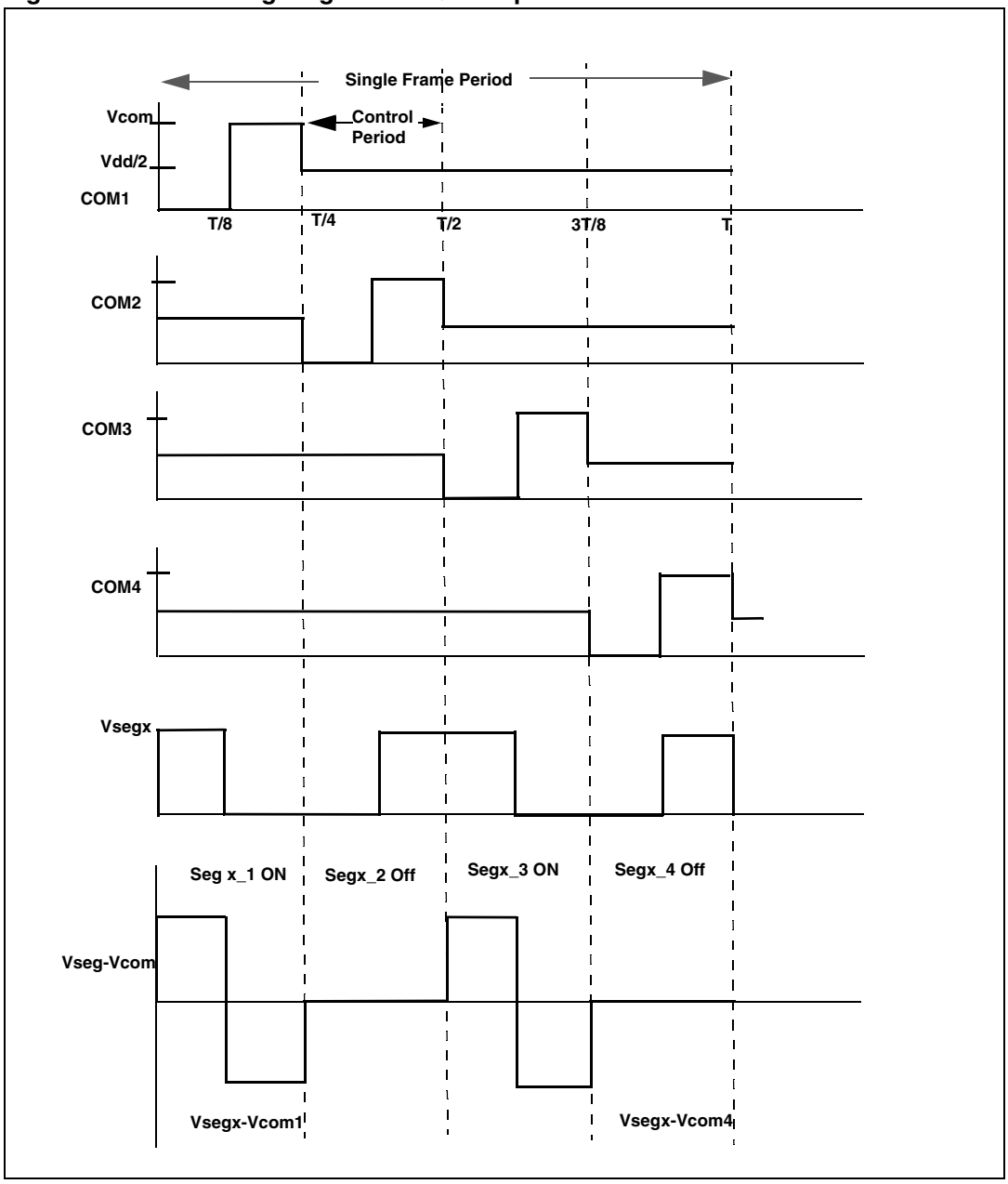
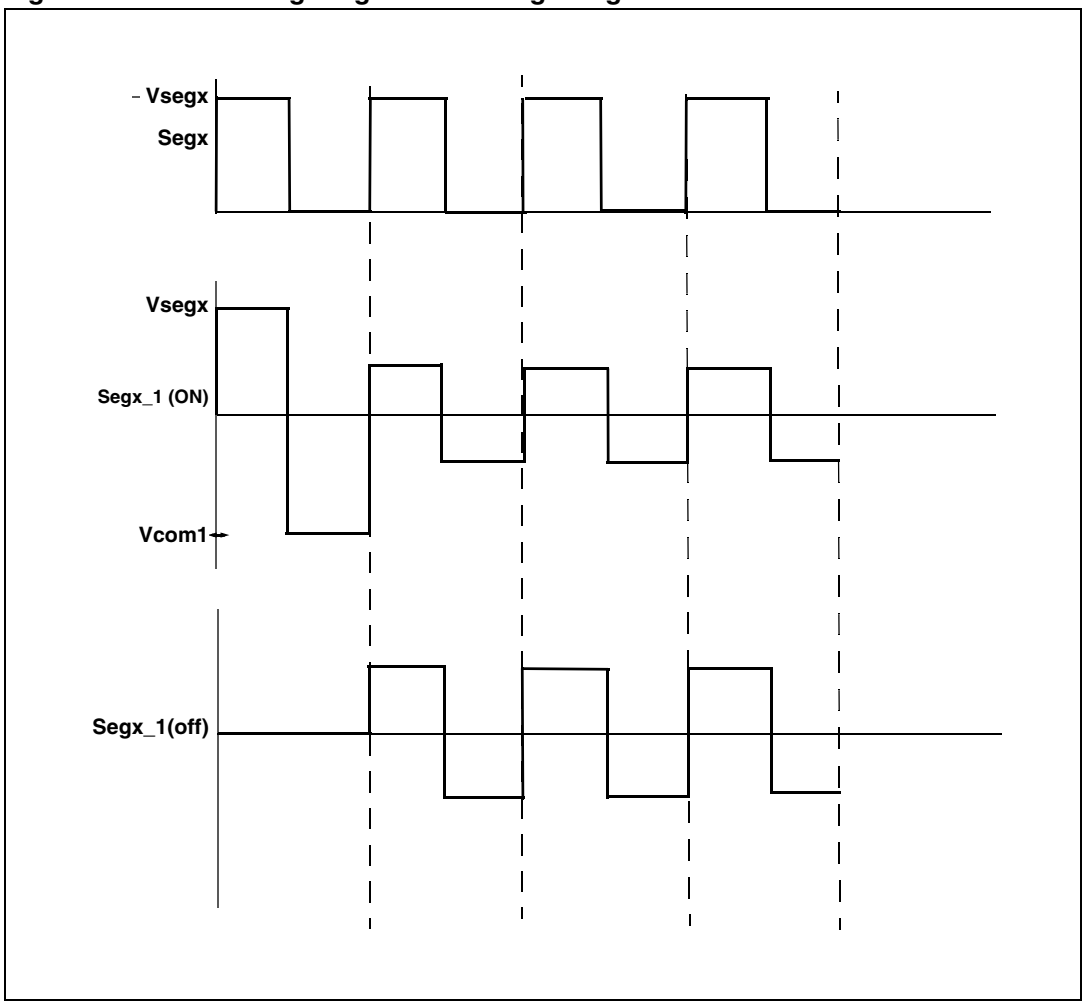


**Figure 7. LCD Timing Diagram for a single segment**




### 2.3.1 LCD mean voltage calculation

The LCD mean voltage must be very close to zero to guarantee long life to the LCD. The LCD mean voltage for ON and OFF periods can be calculated as:

Vmean(ON) = 1/8 Vseg + 1/8 (-Vcom) + 3(Vseg - Vr/2) + 3(-Vr/2) ----(1)

Vmean(Off) = 3(Vseg/2) + 3(-Vr/2) -----(2)

Vmean(ON) and Vmean(Off) assume identical periods for each phase.

From eqn (1) & (2), to get Vmean(ON) and Vmean(Off) = zero

Vseg = Vcom = Vr = Vcc

Where:

Vcom = Max voltage on COM line

Vr/2 = Voltage in the middle of the resistor bridge applied on the COM line

Vseg = Max voltage on Segx line

Vcc = Microcontroller power supply

### 2.3.2 Contrast calculation

The performance of an LCD driving system is defined by the contrast:

$$\text{Contrast}(D) = \text{Vrms}(ON) / \text{Vrms}(Off)$$

For the quadruplex signal as described on the previous page:

$$\text{Vrms}(ON) = \sqrt{\frac{1}{T}\int_0^T f(t)^2 dt}$$

$$\text{Vrms}(ON) = \sqrt{\frac{1}{T}\left(\int_0^{\frac{T}{8}} (Vcc)^2 dt + \int_{\frac{T}{8}}^{\frac{2T}{8}} (Vcc)^2 dt + \int_{\frac{2T}{8}}^{T} \left(\frac{Vcc}{2}\right)^2 dt\right)}$$

$$\text{Vrms}(ON) = \sqrt{\frac{1}{T}\left((Vcc)^2 \cdot \frac{T}{8} + (Vcc)^2 \cdot \frac{T}{8} + \frac{(Vcc)^2}{4} \cdot (6T)/8\right)}$$

$$\text{Vrms}(ON) = \sqrt{\frac{7}{16}(Vcc)^2}$$

$$\text{Vrms}(ON) = 0.661 Vcc$$

$$\text{Vrms}(OFF) = \sqrt{\frac{1}{T}\left(\int_0^{\frac{T}{8}} (0) dt + \int_{\frac{T}{8}}^{\frac{2T}{8}} (0) dt + \int_{\frac{2T}{8}}^{T} \left(\frac{Vcc}{2}\right)^2 dt\right)}$$

$$\text{Vrms}(OFF) = \sqrt{\frac{3}{16}(Vcc)^2}$$

$$\text{Vrms}(OFF) = 0.43 Vcc$$

$$\text{Contrast}(D) = \text{Vrms}(ON) / \text{Vrms}(OFF) = 0.661 Vcc / 0.43 Vcc = 1.52$$

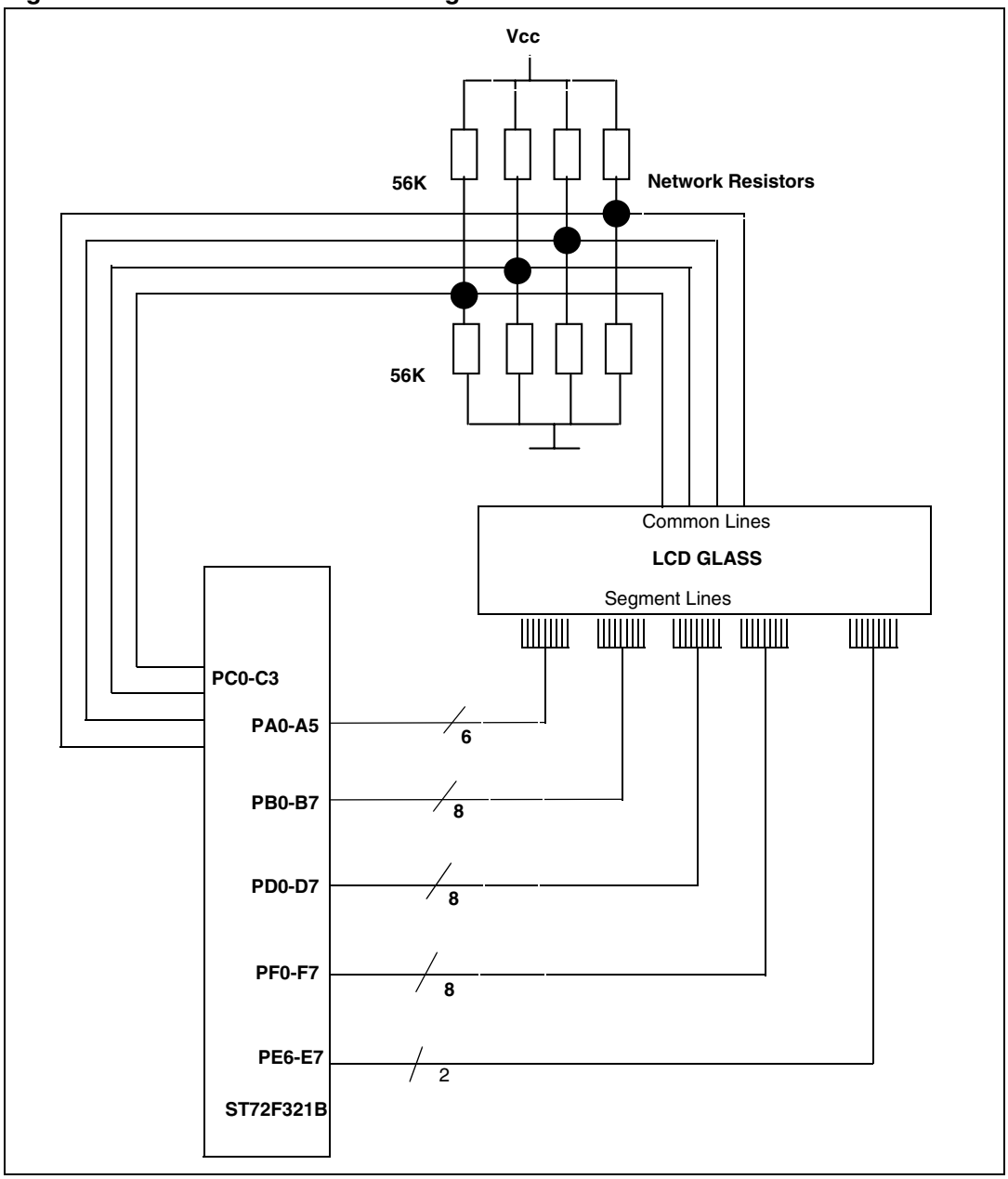
For comparison, a hardware LCD drive uses 1/3 bias voltage. With 1/3 bias control, the contrast value (D) is **1.73**. Therefore, 1/3 bias gives only a small advantage of contrast versus temperature. This advantage is reduced to zero when using software contrast control.

# 3 Example of a quadruplex LCD with ST72F321B

The following example describes a drive for a quadruplex mode (4COM) LCD using the ST72F321B (TQFP64 pin package 10 x 10). Refer to *Figure 8*. The only external components needed for driving the LCD are eight resistors. The resistor value of 56K is used to reduce the DC voltage on the LCD(~7.5 mV). This value can be further decreased to get the better DC voltage on the LCD but this will result in an increase of the current consumption. One I/O port per segment and one I/O port for each COM line are needed to drive the LCD. For example: To drive a quadruplex LCD that has 128 segments (with 32 segment lines and 4 COM lines) requires only a total of 36 I/O ports.

In the example program, the Port PA0-A5, PB0-B7, PD0-D7, PF7-F0, PE7-E6 pins are connected to the 32 segment lines and are used to generate the segment signals. Ports PC3...PC0 are connected to the 4 COM lines and used to generate the COM signals. The LCD driver consists of two initialization routines (port init, timer init) and a TimerA interrupt routine “timer_rt”. To activate the LCD, these two initialization routines have to be called. After these routines are called, the ST7 gets the timer Output Compare 1 & Output Compare 2 interrupts.

**Figure 8. Hardware Connection Diagram**




The LCD Timing is generated by the TimerA output compare interrupt. Each cycle consists of four phases, one for each backplane. Each COM line generates its waveform during the corresponding phase e.g. COM1 line during phase1. During other phases it remains at level $V_{DD}/2$. Each phase consists of two parts:

1. Active time
2. Dead time

During the Active time, the segment lines and COM lines are used to drive the LCD. During dead time Segment and COM lines are used to tune the contrast.

Active time starts after the Output Compare 1 interrupt and dead time starts after the Output Compare 2 interrupt. A total of 16 interrupts are generated in each frame period with four interrupts per control period. There are 2 Output Compare 1 events (OC1_1 and OC1_2) and 2 Output Compare 2 events in each phase.These are explained as follows:

During OC1_1, $V_{DD}$ is applied to the segments which have to be turned ON and 0 for the segments which have to be turned OFF. The COM line which corresponds to this phase is set to low level. Other COM lines are set to level $V_{DD}/2$.

During OC2, all segments and COM lines are inactive (set to low level) if we want to decrease the Vrms (see *Figure 9*) and COM lines are set low, segments are set high if we want to increase the Vrms (see *Figure 10*).

During OC1_2, Segment Lines are supplied with voltage levels which are inverted to the one applied during OC1_1.COM line which corresponds to this phase is set to high level.Other COM lines are set to level $V_{DD}/2$.

Again during OC2, all segments and COM lines are inactive(set to low level) if we want to decrease the Vrms and COM lines are set high, segments are set low if we want to increase the Vrms (see *Figure 10*).

**Figure 9. LCD timing diagram with Dead & Active Time (to decrease Vrms)**

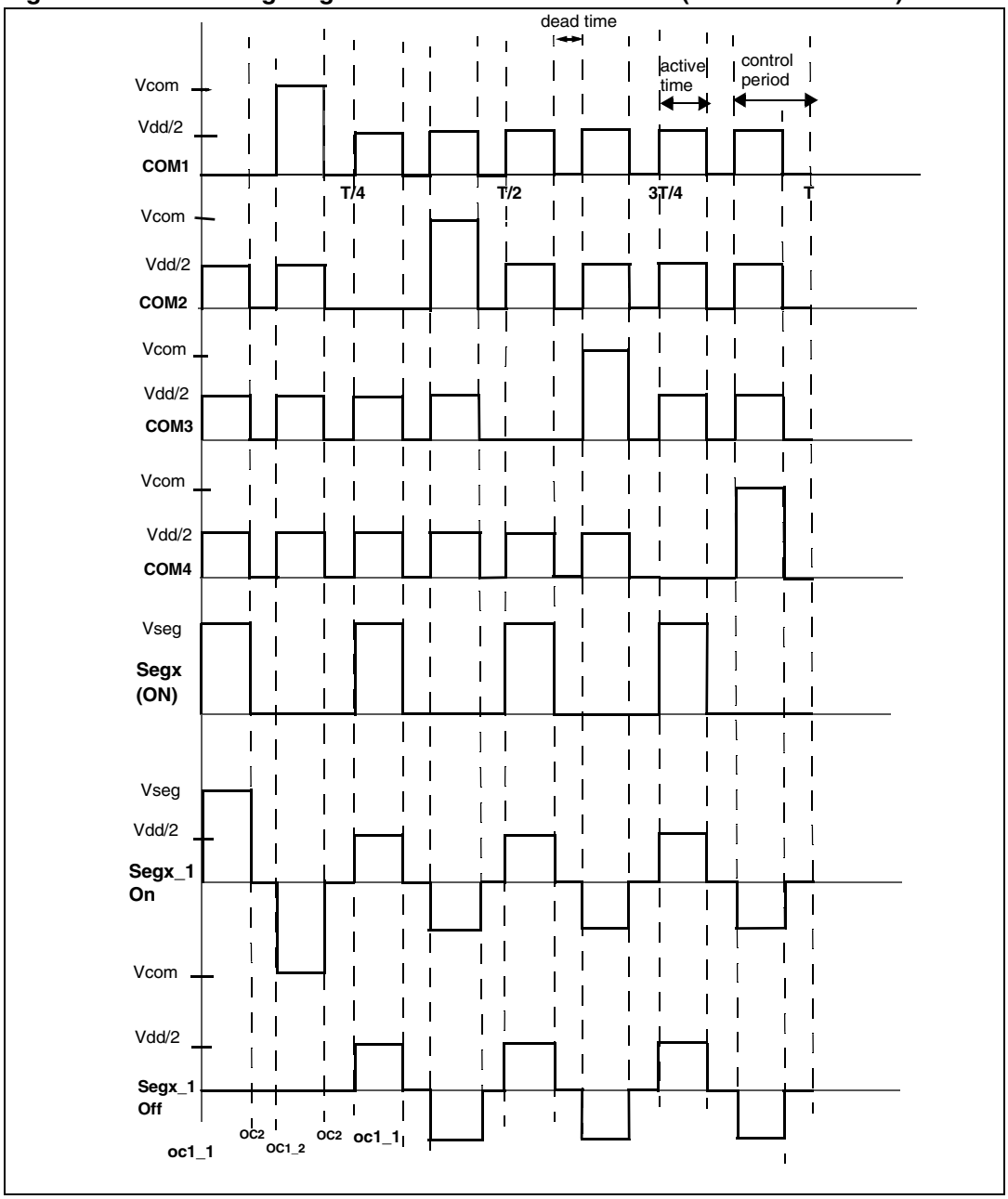
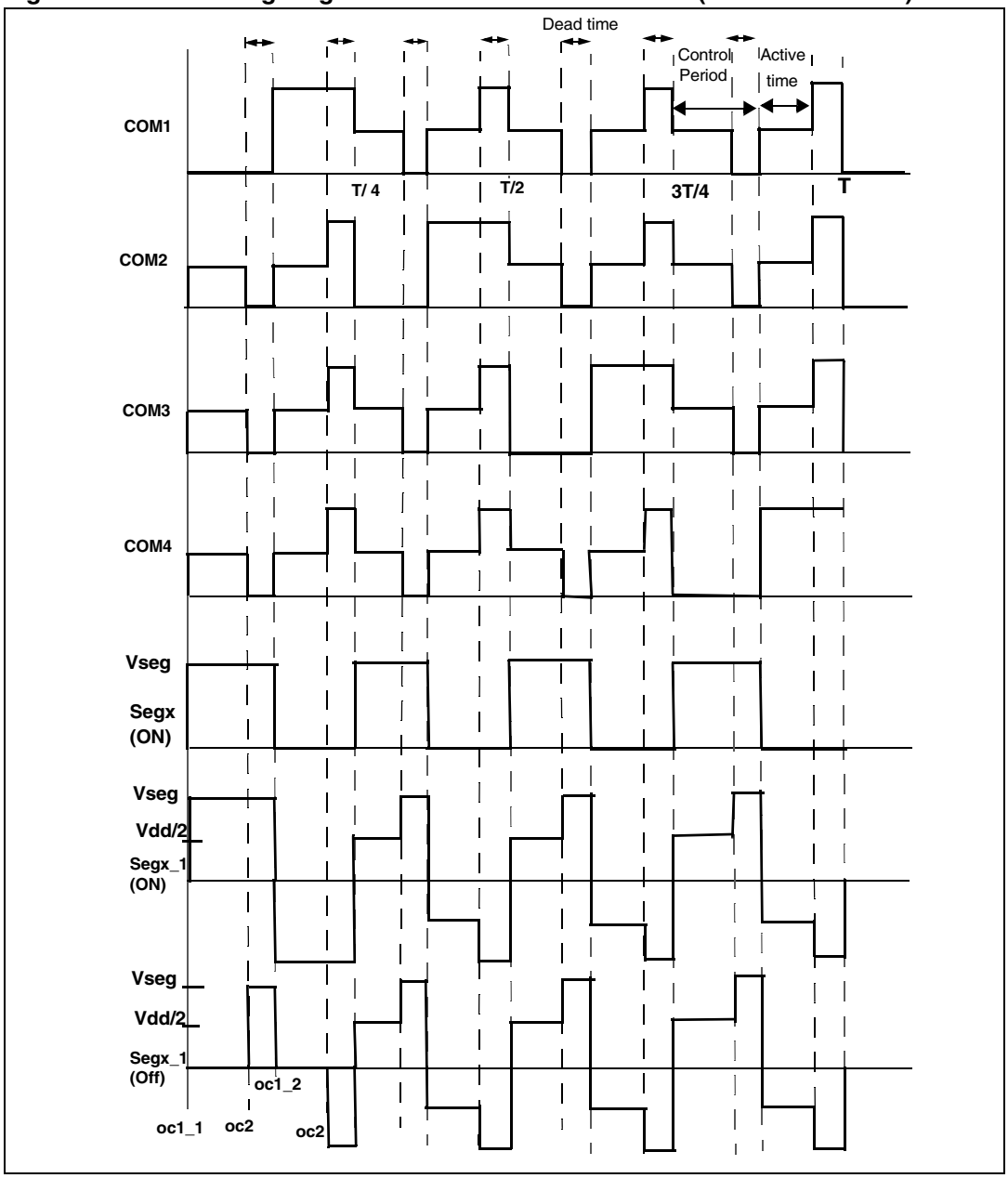


**Figure 10. LCD timing diagram with Active and dead time (to increase Vrms)**



# 4 Software contrast control

The software contrast control is under pending patent from STMicroelectronics. The use of this technique with a non-STMicroelectronics' Microcontroller has to be agreed by STMicroelectronics.

The LCD contrast is controlled entirely by software without the use of any external components. LCD contrast can be adjusted to the optimal value depending on the operating voltage of the LCD used. The LCD contrast is controlled by varying the timing of dead phase as shown in the LCD timing diagram.

Deadtime can be used to decrease as well as to increase the Vrms of the LCD. Deadtime is the voltage compensation time to regulate rms voltage up and down. Dead time can be implemented either after each control period or at the end of the frame. To avoid flickering, the duration of the dead time must be adjusted depending on the quality of LCD and the frequency of the frame.

In the example in *Figure 9*, the Rms value of the LCD decreases if the duration of dead time is increased and Rms value increases if the duration of dead time decreases. In *Figure 10*, this works the opposite way.

## 4.1 Contrast calculations

Let the frame period = T + xT

where T - Active Time, xT- Dead Time

x- Proportion of dead time, Vx - Voltage during the dead time

$$Vrms(ON) = \sqrt{\frac{1}{T + xT}\int_0^{(T + XT)} f(t)^2 dt}$$

$$Vrms(ON) = \sqrt{\frac{1}{T + xT}\left(\int_0^{\frac{T}{8}} (Vcc)^2 dt + \int_{\frac{T}{8}}^{\frac{2T}{8}} (-Vcc)^2 dt + \int_{\frac{2T}{8}}^{T} ((Vcc)/2)^2 dt + \int_0^{\frac{xT}{8}} (Vx^2) dt \cdot 8\right)}$$

$$Vrms(ON) = \sqrt{\frac{1}{T + xT}\left((Vcc)^2 \cdot \frac{T}{8} + (Vcc)^2 \cdot \frac{T}{8} + \frac{(Vcc)^2}{4} \cdot \frac{2T}{8} + \left(Vx^2 \cdot \frac{xT}{8}\right) \cdot 8\right)}$$

$$Vrms(ON) = \sqrt{\frac{1}{1+x}\left(\frac{(14Vcc^2)}{32} + (Vx)^2 \cdot x\right)}$$

Since Vx = 0 (incase of a decrease in Vrms)

$$Vrms(ON) = \sqrt{\frac{1}{1+x}\frac{(14Vcc^2)}{32}}$$

$$Vrms(ON) = \sqrt{\frac{1}{1+x}}0.661Vcc$$

$$Vrms(OFF) = \sqrt{\frac{1}{T+xT}\left(\int_0^{\frac{T}{8}}(0)dt + \int_{\frac{T}{8}}^{\frac{2T}{8}}(0)dt + \int_{\frac{2T}{8}}^{T}((Vcc)/2)^2 dt + \int_0^{\frac{xT}{8}}(Vx^2)dt \cdot 8\right)}$$

$$Vrms(OFF) = \sqrt{\frac{1}{1+x}\left(\frac{(6Vcc^2)}{32} + Vx^2 \cdot x\right)}$$

Since Vx = 0 (incase of a decrease in Vrms)

$$Vrms(OFF) = \sqrt{\frac{1}{1+x}}0.18Vcc$$

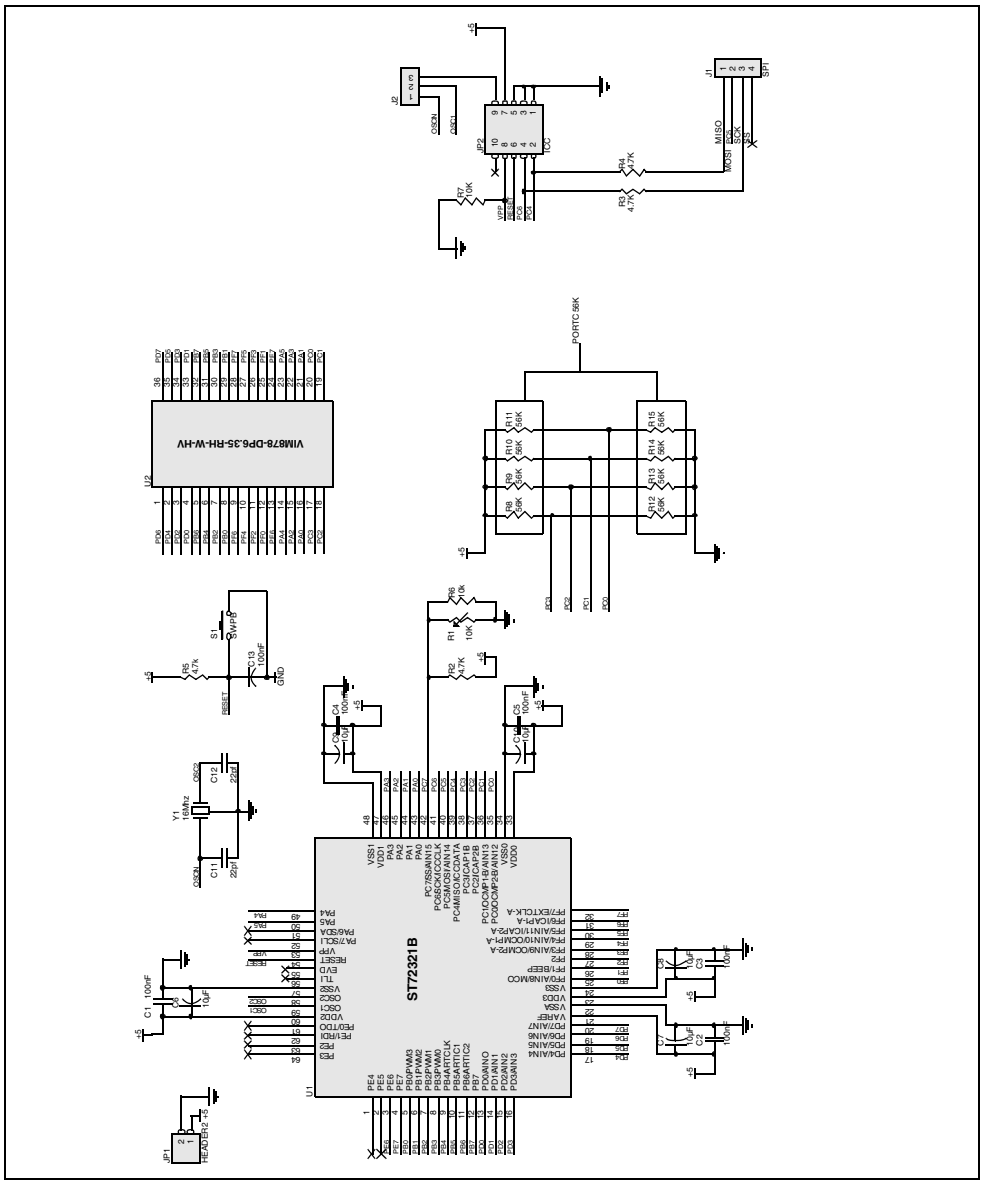
$$Contrast(Dx) = \frac{\left(\sqrt{\frac{1}{1+x}}0.661Vcc\right)}{\left(\sqrt{\frac{1}{1+x}}0.18Vcc\right)}$$

Where Dx = Contrast calculation with contrast control method

The contrast D, between $V_{ON}$ and $V_{OFF}$ is constant (quality of contrast). We only change the optical contrast by tuning $V_{ON}$ close to the threshold value of the LCD.

# 5 LCD demo board

## 5.1 Schematic



## 5.2 Power supply

The LCD demo board should be supplied by a maximum DC voltage of 5V. The board is provided with the connector JP1 for this board supply.

*Note: For the demo software loaded inside the micro, the board should be supplied with 5V. The software attached to this application note displays the word "EMBEDDED" and tunes automatically its contrast from transparent to dark with the ST software pattented method. The Vrms increase is performed by putting the segment voltage once at Vdd, once at -Vdd during the dead times, the Vrms decrease is performed by putting at 0 the segment voltage during the same dead times. The voltage average is then kept. Refer to the software attached to this application note for more details.*

## 5.3 Programming

The demo board uses the ST72F321B microcontroller and can be programmed using the ICC protocol. The board is provided with the ICC connnector JP2. By default, OSC_TYP is programmed as a resonator oscillator in the option bytes. You can disable the option bytes when you want to use the ICC clock to program the micro.

## 5.4 Reset

The device can be reset by pressing the switch s1 on the demo board.

## 5.5 Oscillation system

The demo board is mounted with a 16 MHz crystal with 8 MHz fcpu. You can change this clock value but need to modify the timer setting inside the software accordingly.

# 6 Revision history

**Table 1. Document revision history**

| Date | Revision | Changes |
|---|---|---|
| 09-May-2006 | 5 | Document reformatted<br>References to ST72F321 changed to ST72F321B<br>Formulae for VRMS(ON) and VRMS(OFF) corrected, *Section 4.1 on page 16*<br>Note updated, *Section 5.2 on page 19* |

**Please Read Carefully:**

Information in this document is provided solely in connection with ST products. STMicroelectronics NV and its subsidiaries (“ST”) reserve the right to make changes, corrections, modifications or improvements, to this document, and the products and services described herein at any time, without notice.

All ST products are sold pursuant to ST’s terms and conditions of sale.

Purchasers are solely responsible for the choice, selection and use of the ST products and services described herein, and ST assumes no liability whatsoever relating to the choice, selection or use of the ST products and services described herein.

No license, express or implied, by estoppel or otherwise, to any intellectual property rights is granted under this document. If any part of this document refers to any third party products or services it shall not be deemed a license grant by ST for the use of such third party products or services, or any intellectual property contained therein or considered as a warranty covering the use in any manner whatsoever of such third party products or services or any intellectual property contained therein.

**UNLESS OTHERWISE SET FORTH IN ST’S TERMS AND CONDITIONS OF SALE ST DISCLAIMS ANY EXPRESS OR IMPLIED WARRANTY WITH RESPECT TO THE USE AND/OR SALE OF ST PRODUCTS INCLUDING WITHOUT LIMITATION IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE (AND THEIR EQUIVALENTS UNDER THE LAWS OF ANY JURISDICTION), OR INFRINGEMENT OF ANY PATENT, COPYRIGHT OR OTHER INTELLECTUAL PROPERTY RIGHT.**

**UNLESS EXPRESSLY APPROVED IN WRITING BY AN AUTHORIZE REPRESENTATIVE OF ST, ST PRODUCTS ARE NOT DESIGNED, AUTHORIZED OR WARRANTED FOR USE IN MILITARY, AIR CRAFT, SPACE, LIFE SAVING, OR LIFE SUSTAINING APPLICATIONS, NOR IN PRODUCTS OR SYSTEMS, WHERE FAILURE OR MALFUNCTION MAY RESULT IN PERSONAL INJURY, DEATH, OR SEVERE PROPERTY OR ENVIRONMENTAL DAMAGE.**

Resale of ST products with provisions different from the statements and/or technical features set forth in this document shall immediately void any warranty granted by ST for the ST product or service described herein and shall not create or extend in any manner whatsoever, any liability of ST.

ST and the ST logo are trademarks or registered trademarks of ST in various countries.

Information in this document supersedes and replaces all information previously supplied.

The ST logo is a registered trademark of STMicroelectronics. All other names are the property of their respective owners.

© 2006 STMicroelectronics - All rights reserved

STMicroelectronics group of companies

Australia - Belgium - Brazil - Canada - China - Czech Republic - Finland - France - Germany - Hong Kong - India - Israel - Italy - Japan - Malaysia - Malta - Morocco - Singapore - Spain - Sweden - Switzerland - United Kingdom - United States of America

**www.st.com**